

TRANSITION SYSTEM TO LOW POWER CONSUMPTION STATE

Patent Number: JP62150416

Publication date: 1987-07-04

Inventor(s): KADOTA HIROSHI

Applicant(s):: NEC CORP

Requested Patent: JP62150416

Application Number: JP19850295114 19851224

Priority Number(s):

IPC Classification: G06F1/00 ; G06F9/46 ; G06F15/06

EC Classification:

Equivalents:

Abstract

PURPOSE: To eliminate the disturbance of other task execution by bringing the computer system to the standby mode when the absence of a task to be executed is detected in the system applying multi-task processing.

CONSTITUTION: A computer system is added with a program memory 1, a program counter (PC) 2, an instruction decoder 3, a peripheral equipment 4, a clock generator 5, a data memory 6, a decision circuit 7, an AND gate 8 and a latch 21 with inverter, the instruction decoder 3 activates each signal line for the system operation. In this case, a clock is fed to the peripheral equipment 4 and the PC 2 via the AND gate 8 and when the output 20 of the latch 21 is inactive, the mode is brought into the standby mode where the peripheral equipment 4 is stopped. Further, the standby mode continues until the latch state is released.

Data supplied from the esp@cenet database - I2